© INTERNATIONAL JOURNAL FOR RESEARCH PUBLICATION & SEMINAR
ISSN: 2278-6848 | Volume: 07 Issue: 09 | October – December 2016
Paper is available at www.jrps.in | Email : info@jrps.in

# Analysis Of Low Power Techniques For VLSI Circuit

1NEERAJ CHOUDHARY, 2SHIPRA SHARMA ,
1Research Scholar, Department of Electronics and communication, CBS Groups of Institutions
2HOD. Department of Electronics and Communication, CBS Groups of Institutions

**Abstract**:-This paper, presents a concept of the power optimization theory approach , the estimation techniques and Power consumption is very important issue in VLSI circuit in recent days and power dissipation has become concern for VLSI circuit designers with increase in number of chip. According to MOORE'S in every decade the number of chip is double. So power dissipation is became top challenge in ITRS report roadmap for semiconductor. Speed is second key factor. With advancement of technology everyone wants high speed devices with long power backup. But static and dynamic leakage current results in higher leakage power which reduces the power backup of portable devices.


The main objective of dissertation is to reduce the power consumption of the circuit by using different design techniques. These techniques are sleep, stack, sleep keeper and leakage feedback technique. All these techniques are used for XNOR gate and 1-bit full adder.

A 28T 1-bit full adder is designed on cadence using 180nm technology using all techniques and analyzed the leakage power for the circuit. An 8T XNOR gate also designed on 180nm technology by using all above techniques and leakage power is analyzed. Delay, which reduces the speed of circuit is also analyzed for all above maintained technique.

**Introduction**:-Power consumption is very important issue in VLSI circuit in recent days. With increase in number of transistors in VLSI circuit we need devices which have lesser power consumption and short delay. But power consumption and delay are contradictory to each other. As supply voltage is lowered to reduce power dissipation, threshold voltage is also lowers to maintain performance of circuit. So for better performance of circuit, it is essential to have smaller threshold voltage. Due to scaling down of threshold voltage the sub threshold current increases linearly which increases leakage current.

Leakage power dissipation is now one of the most critical issues in designing low power VLSI circuits. In this paper various techniques like sleep approach, stack approach, sleepy keeper has

© INTERNATIONAL JOURNAL FOR RESEARCH PUBLICATION & SEMINAR
ISSN: 2278-6848 | Volume: 07 Issue: 09 | October – December 2016
Paper is available at www.jrps.in | Email : info@jrps.in

been discussed to low the power dissipation in the VLSI circuit. With reduced in the chip size area in VLSI circuits transistors packing is more so it is important to design low power VLSI circuit so less power dissipation is occurs.

Two type of power consumption are occurred in CMOS circuit one is dynamic power and other is static power. Dynamic power consumption is occurs when switching of the transistor is take place, and static power consumption is not independent of switching of transistor. Dynamic power was previously at 180nm technology and above circuit is the single largest concern for low-power chip designers since dynamic power accounted for 90% or more of the total chip power. Thus most of the research and work has been done previously which focus on the dynamic power reduction. However, as feature size shrinks to 90nm to 65 nm, static power has become a great challenge for current and future technologies.

**Power Consumption**:-Power consumption of CMOS circuit is mainly consists of two things, one is dynamic power consumption and another one is static power consumption. Dynamic power consumption is known as a switching power consumption that happened when the transistor is in working mode, but however static power consumption means regardless of transistor switching. Although it is not the concern for VLSI circuit designer when the technology size was 180nm or above, but when the technology feature size was shrink means below 130nm, then static power consumption become the dominant factor in total power consumption of chip.

The average power consumption of CMOS can be modeled with the following equation

$$P_{Avg} = P_{Dynamic} + P_{Static} \quad (1)$$

The dominate part of $P_{Avg}$ is the dynamic power, $P_{Dynamic}$, caused by $P_{Switching}$ and $P_{Short-circuit}$. $P_{Switching}$ can be expressed by the following equation

$$P_{Switching} = K \cdot C_{out} \cdot V_{dd} \cdot V_{swing} \cdot f \quad (2)$$

Where, the node transition activity factor K, load capacitance $C_{out}$, supply voltage $V_{dd}$, and working frequency f.

**Dynamic Power**:-Dynamic power dissipation is caused by switching activities of the circuit. A higher operating frequency leads to more frequent switching activities in the circuits and results

© INTERNATIONAL JOURNAL FOR RESEARCH PUBLICATION & SEMINAR
ISSN: 2278-6848 | Volume: 07 Issue: 09 | October – December 2016
Paper is available at www.jrps.in | Email : info@jrps.in

in increased power dissipation. The most significant source of dynamic power dissipation in CMOS circuits is the charging and discharging of capacitors. CMOS circuit dynamic power consumption equation can be written as:

$$P_{Dynamic} = C V^2_{DD} f \quad (3)$$

Where, f is frequency of input signal frequency, C is the switched capacitance, V is supply voltage.

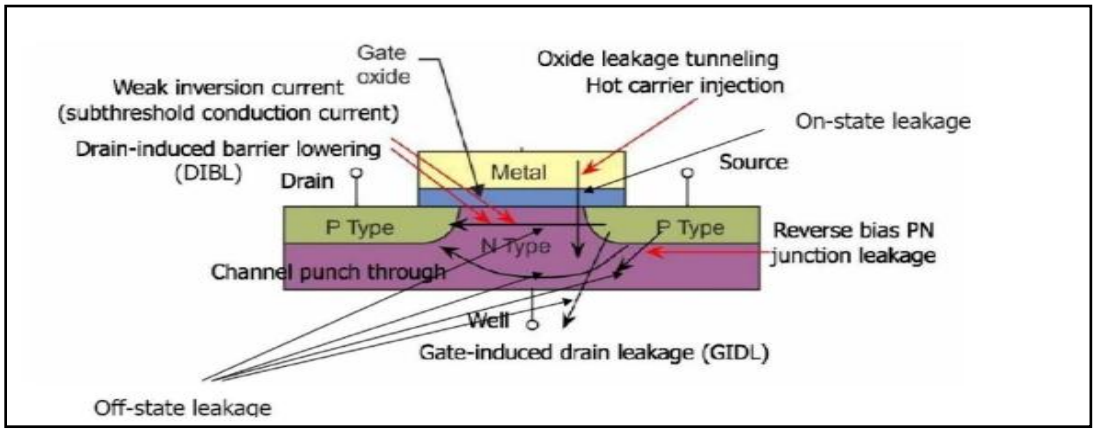
**Static Power:-**The static or steady state power dissipation of a circuit depends upon logical state of circuit rather than switching activities and is expressed as:

$$P_{Static} = I_{Static}.V_{DD} \quad (4)$$

Where, $I_{Static}$ is the current that flows through the circuit when there is no switching activity. Ideally, CMOS circuits dissipate no static (DC) power as in steady state there is no direct path from $V_{DD}$ to ground because PMOS and NMOS transistors are never becomes on simultaneously. Therefore static power dissipation is due to leakage currents and substrate injection currents.

There are many reasons for which power losses occur in CMOS circuit. Fig. 1 shows different types of leakage components. They are:

1. Sub-threshold leakage (weak inversion current)
2. Gate oxide leakage (tunneling current)
3. Channel punch through
4. Drain induced barrier lowering



© INTERNATIONAL JOURNAL FOR RESEARCH PUBLICATION & SEMINAR
ISSN: 2278-6848 | Volume: 07 Issue: 09 | October – December 2016
Paper is available at www.jrps.in | Email : info@jrps.in

**Fig 1: Leakage power components in CMOS**

One of the main reasons causing the leakage power increase is increase of sub-threshold leakage power. The Sub-threshold conduction or the sub-threshold leakage or the sub-threshold drain current is the current that flows between the source and drain of a MOSFET when the transistor is in sub-threshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage. The sub-threshold region is often referred to as the weak inversion region. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases which increases the sub-threshold leakage power. Next the gate oxide leakage, the gate oxide, which serves as insulator between the gate and channel, should be made as thin as possible to increase the channel conductivity and performance. But as the gate oxide is made thinner the barrier voltage of the oxide changes. For the positive gate voltage thus some positive charges get stuck in the oxide. Therefore, current flows through the oxide. This is also known as tunneling Current.

Punch through in a MOSFET is an extreme case of channel length modulation where the depletion layers around the drain and source regions merge into a single depletion region. The field underneath the gate then becomes strongly dependent on the drain-source voltage, as is the drain current. Punch through causes a rapidly increasing current with increasing drain-source voltage. This effect is undesirable as it increases the output conductance and limits the maximum operating voltage of the device.

Drain induced barrier lowering or DIBL is referred to the reduction of threshold voltage of the transistor at higher drain voltages. The combined charge in the depletion region of the device and that in the channel of the device is balanced by three electrode charges: the gate, the source and the drain. As drain voltage is increased, the depletion region of the p-n junction between the drain and body increases in size and extends under the gate, so the drain assumes a greater portion of the burden of balancing depletion region charge, leaving a smaller burden for the gate. As a result, the charge present on the gate retains charge balance by attracting more carriers into the channel, an effect equivalent to lowering the threshold voltage of the device.

© INTERNATIONAL JOURNAL FOR RESEARCH PUBLICATION & SEMINAR
ISSN: 2278-6848 | Volume: 07 Issue: 09 | October – December 2016
Paper is available at www.jrps.in | Email : info@jrps.in

The reverse bias diode leakage occur when a transistor is turned off and another active transistor charges up/down the drain with respect to former's bulk potential[12] [18]. For example, consider an inverter with a high input voltage, in which the NMOS transistor is turned on and the output voltage is driven low. The PMOS transistor will be turned off, but its drain-to-bulk voltage will be equal to $-V_{DD}$ since the output is at 0 V and the bulk for PMOS is at $V_{DD}$.

Speed of operation of a digital system is determined by the propagation delay of the logic gates used to construct the system.

**Propagation Delay:** The delay measured from the time the input is at 50% of its full swing value to the time the output reaches its 50% value**.** It determines input to output signal delay during high to low and low to high transitions of output.

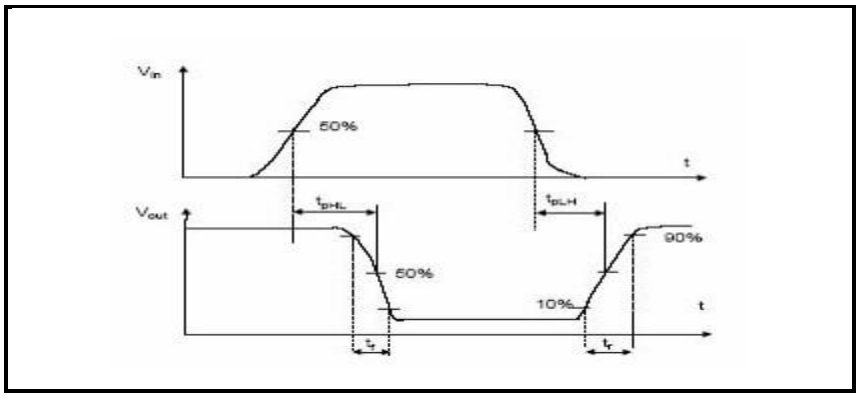
- **High to Low ( $\acute{I}_{PHL}$ ):** It is the time delay between the $V_{50\%}$ transition of the rising input voltage and the $V_{50\%}$ transition of the falling output voltage.
- **Low to High ( $\acute{I}_{PLH}$):** It is the time delay between the $V_{50\%}$ transition of the falling input voltage and the $V_{50\%}$ transition of the rising output voltage.

$$\acute{I}_{PHL} = 1.6*C/ [K_n* (W/L)*V_{DD}] \quad (5)$$

Where C is Capacitance, $V_{DD}$ is supply voltage and $K_n*(W/L)$ is transconductance.

$$\acute{I}_P = (\acute{I}_{PHL} + \acute{I}_{PLH})/2 \quad (6)$$

Where, $\acute{I}_P$is propagation delay.



© INTERNATIONAL JOURNAL FOR RESEARCH PUBLICATION & SEMINAR
ISSN: 2278-6848 | Volume: 07 Issue: 09 | October – December 2016
Paper is available at www.jrps.in | Email : info@jrps.in

**Fig. 2: Propagation delays and rise and fall time graph of Output w.r.t Input**

**Circuit Timing Parameters**

- **Rise Time:** It is defined as time required for a output voltage to rise from $V_{10\%}$ value to $V_{90\%}$ level.
- **Fall Time:** It is defined as time required for output voltage to drop from $V_{90\%}$ to $V_{10\%}$ value.

## Result:-

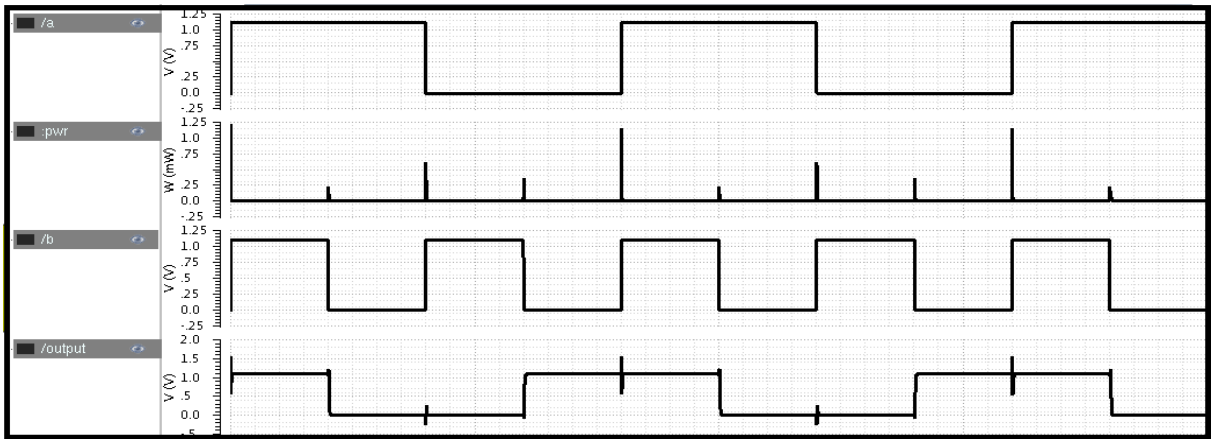



**Fig 3: Transient Response of XNOR using Leakage feedback technique**

Transient analysis of XNOR gate is show in above graph which is designed on 180nm technology on Cadence tool. The graphs shows power and output of XNOR gate with respect to the input provided at the gate. From this analysis we calculate power, delay and power delay product which is listed in Table 1.

| **Parameters** | **Values** |
|---|---|
| Power | 2.2 µW |
| Delay | 19.95 ns |

© INTERNATIONAL JOURNAL FOR RESEARCH PUBLICATION & SEMINAR
ISSN: 2278-6848 | Volume: 07 Issue: 09 | October – December 2016
Paper is available at www.jrps.in | Email : info@jrps.in

| | |
|---|---|
| Power Delay Product | 43.23 fJ |

**Table 1: Power, delay and PDP of XNOR using leakage feedback technique**

XNOR gate is simulated on cadence at 180nm technology using all power lowering techniques. Result obtained after simulation are listed in table 2.

| **Parameter** | **Basic XNOR** | **Sleep technique** | **Stack technique** | **Sleep-keeper technique** | **Leakage feedback technique** |
|---|---|---|---|---|---|
| Average Power(µW) | 2.2 | 1.65 | 1.82 | 2.01 | 2.15 |
| Delay(ns) | 19.95 | 10.15 | 10.19 | 10.10 | 10.22 |
| Power delay product(fJ) | 43.23 | 16.65 | 18.54 | 20.3 | 21.97 |

**Table 2: Comparison of Average power, delay and PDP of different techniques**

From the table 2 it is observed that all the power lowering techniques have less power consumption than the basic XNOR gate. Delay and power delay product also reduced comprehensively.

Parametric analysis of full adder using sleep keeper technique has been simulated on basis of different temperature and voltage. Above graph is taken on different temperature ranging from -20 to 120. Voltage is also a parameter for this analysis and it is ranging from 0.4 to 1.1 V. Graph is shown in fig 4 .

© INTERNATIONAL JOURNAL FOR RESEARCH PUBLICATION & SEMINAR
ISSN: 2278-6848 | Volume: 07 Issue: 09 | October – December 2016
Paper is available at www.jrps.in | Email : info@jrps.in

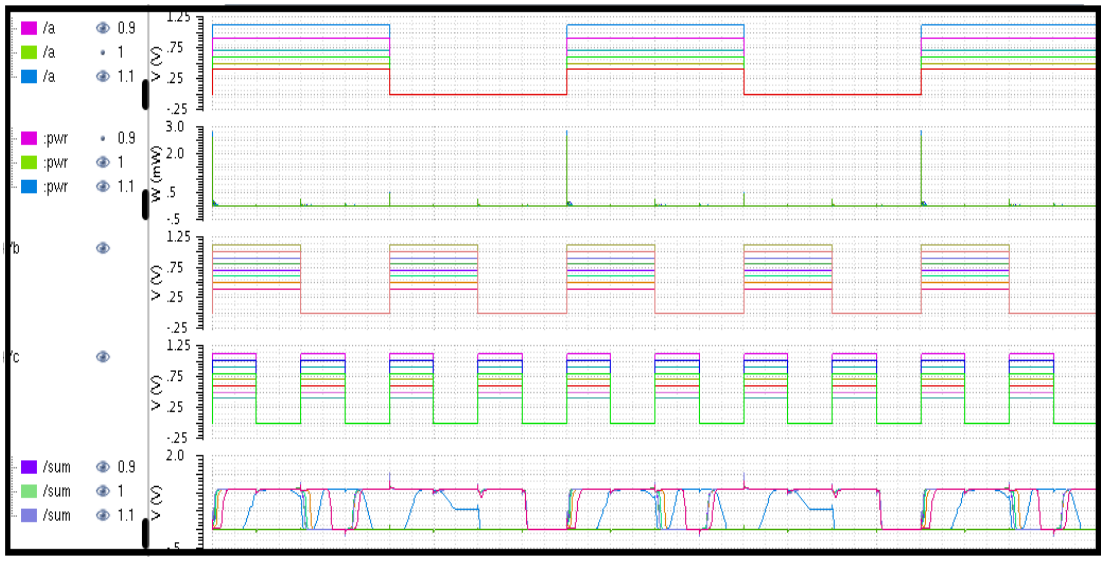



**Fig 4: Parametric analysis of full adder using sleep keeper at different voltage**

A 28T 1-bit full adder has been simulated on cadence tool using 180nm technology. Transient analysis of full adder using different techniques has been studied and results obtained are listed below in table 3.

| **Parameter** | **Basic** | **Sleep technique** | **Stack technique** | **Sleep keeper technique** | **Leakage feedback technique** |
|---|---|---|---|---|---|
| Average Power(µW) | 6.75 | 4.711 | 5.134 | 4.911 | 6.55 |
| Delay (ns) | 19.84 | 20.01 | 19.77 | 20.03 | 19.77 |
| Power delay product(fJ) | 133.92 | 95.44 | 101.49 | 98.22 | 129.49 |

**Table 3: Comparison of average power, delay and PDP for full adder**

From the table 3 it is observed that the power consumption in full adder using sleep technique is lowest among the all other techniques used in dissertation. However delay is increase as compare to basic circuit. Power delay product is reduced comprehensively by using different techniques.

© INTERNATIONAL JOURNAL FOR RESEARCH PUBLICATION & SEMINAR
ISSN: 2278-6848 | Volume: 07 Issue: 09 | October – December 2016
Paper is available at www.jrps.in | Email : info@jrps.in

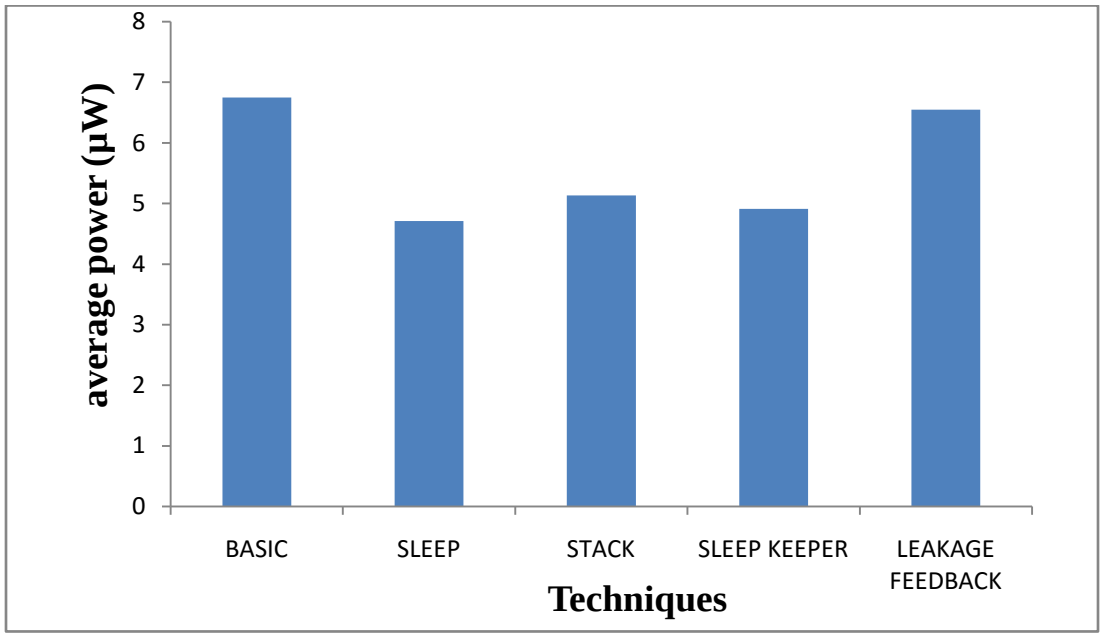



**Fig 5: Comparison of average power of full adder at different techniques**

It is observed from the graph that full adder using sleep technique consume less power. Delay in the all circuit using different techniques almost same the variation in delay can be neglected as it is more efficient in terms of power. The average power obtained for full adder using sleep technique is 4.711µW which is 2.03 µW less then basic full adder. Power delay product graph of full adder is shown in fig 6.

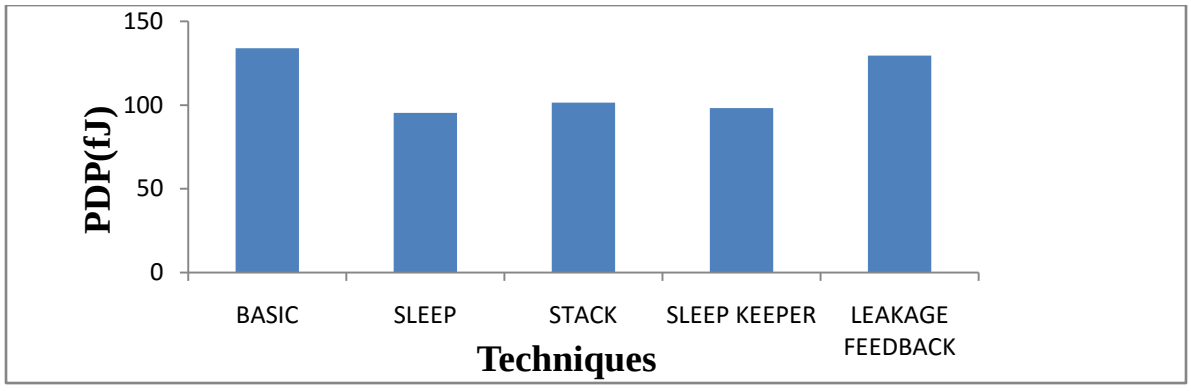



**Fig 6: Power delay product of different techniques for full adder**

**Conclusions**:-In nanometer scale CMOS technology, subthreshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge.The

© INTERNATIONAL JOURNAL FOR RESEARCH PUBLICATION & SEMINAR
ISSN: 2278-6848 | Volume: 07 Issue: 09 | October – December 2016
Paper is available at www.jrps.in | Email : info@jrps.in

XNOR gate circuit and full adder by using different techniques has been designed and simulated on Cadence Virtuoso at 180 nm technology. Though there is a decrease in power in the sleep approach than base case, there is a destruction of state and floating output voltage. In case of sleepy keeper approach, average power is reduced when compared with leakage feedback and stack approach. As we know there is tradeoff between power and delay, sleep technique results in maximum power reduction but with the worst delay. Thus sleep technique shows more than 30% power reduction as compared to normal full adder circuit and for XNOR gate it is 17%. Sleep keeper technique gives power state with a reduced 27% of power in full adder and also overcomes the disadvantage of sleep technique. So, good results were obtained from sleep technique simulation.

- Low power VLSI designs are required to increase the battery life of electronic devices. Hence, circuits with low leakage power design are the future of electronic industry.
- The proposed techniques provide efficient method to reduce power and delay. These techniques will make electronic system more reliable while reducing energy costs.

- In future research could be done to explore design techniques to reduce power and delay as well as area at submicron technology, resulting in overall increase of circuit performance.

With increased market demand for portable consumer electronics powered by batteries and high performance system characterized by large power dissipation, there is going to be much larger need for low power VLSI circuits in future**.**

# REFERENCES

[1]. Dadoria, Ajay Kumar, and KavitaKhare. "A Novel Approach For Leakage Power Reduction Techniques In 65nm Technologies." International Journal of VLSI Design & Communication Systems 5.3 (2014): 1.

[2]. Parveen, Amreen, Amrita Shreevastava, and Mala Kushwah. "Stack Keeper Approach: A Novel Technique To Reduce Leakage Power In CmosVlsi Design." International Journal of Engineering Research and Technology.Vol. 2.No. 3 (March-2013).ESRSA Publications, 2013.

[3]. C. Jagadeesh, R. Nagendra and N. Koppala, "Design & Analysis of Different Types of Sleepy Methods for Future Technologies", IJETI, Volume 4, Issue 4, April 2013

[4]. Deepika, K. Gnana, K. MariyaPriyadarshini, and K. David Solomon Raj. "Sleepy Keeper Approach for Power Performance Tuning in VLSI Design."International Journal of Electronics and Communication Engineering 6.1 (2013): 17-28.

[5]. S Aswale, P., and S. S Chopade. "A low power 90nm technology based CMOS digital gates with dual threshold transistor stacking technique."International Journal of Computer Applications 59.11 (2012): 47-52.

[6]. Kim, Se Hun, and Vincent J. Mooney III. "Sleepy Keeper: a new approach to low-leakage power VLSI design." Very Large Scale Integration, 2006 IFIP International Conference on. IEEE, 2006.

[7]. Raj, Nikhil, and Rohit Lorenzo. "An effective design technique to reduce leakage power." Electrical, Electronics and Computer Science (SCEECS), 2012 IEEE Students' Conference on.IEEE, 2012.

[8]. Barua, Pranabesh. "A novel architecture for nanometer scale low power VLSI design." Computer and Information Technology (ICCIT), 2012 15th International Conference on.IEEE, 2012.

[9]. Priya, M. Geetha, K. Baskaran, and D. Krishnaveni. "Leakage power reduction techniques in deep submicron technologies for VLSI applications."Procedia Engineering 30 (2012): 1163-1170.

[10]. Kim, Se Hun, and Vincent J. Mooney III. "Sleepy Keeper: a new approach to low-leakage power VLSI design." Very Large Scale Integration, 2006 IFIP International Conference on. IEEE, 2006.

[11]. Pal, Pankaj Kr, et al. "New low-power techniques: Leakage Feedback with Stack & Sleep Stack with Keeper." Computer and Communication Technology (ICCCT), 2010 International Conference on.IEEE, 2010.

[12]. Jeon, HeungJun, Yong-Bin Kim, and Minsu Choi. "Standby leakage power reduction technique for nanoscale CMOS VLSI systems." Instrumentation and Measurement, IEEE Transactions on 59.5 (2010): 1127-1133.

[13]. Karmakar, Nittaranjan, et al. "A novel dual sleep approach to low leakage and area efficient VLSI design." Proc. 2009 IEEE Regional Symposium on Micro and Nano Electronics (RSM2009), Kota Bharu, Malaysia. 2009.

[14]. Zhao, Xin, et al. "A novel low-power physical design methodology for MTCMOS." Circuits and Systems, 2006.ISCAS 2006.Proceedings.2006 IEEE International Symposium on.IEEE, 2006.

[15]. Kim, Se Hun, and Vincent John Mooney III. "The Sleepy Keeper Approach: Methodology, Layout and Power Results for a 4-bit Adder." (2006).

[16]. Kim, Nam Sung, et al. "Leakage current: Moore's law meets static power."computer 36.12 (2003): 68-75.

[18]. Kim, N., Austin, T., Baauw, D., Mudge, T., Flaunter, K., Hu, J., Irwin, M., Kandemir, M., And Narayanan, V., “Leakage Current: Moore’s Law Meets Static Power,” IEEE Computer, Vol. 36, Pp. 68-75, December 2003.

[19]. Roy, Kaushik, SaibalMukhopadhyay, and Hamid Mahmoodi-Meimand. "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits." Proceedings of the IEEE 91.2 (2003): 305-327.

[20]. Sri, B. Srujana, et al. "DESIGN OF LOW POWER 4-BIT FULL ADDER USING SLEEPY KEEPER APPROACH." IJRET, NOV (2012).