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HARMONICS ANALYSIS OF A HYBRID ACTIVE NEUTRAL POINT CLAMPED FLYING CAPACITOR FIVE LEVEL INVERTER

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ABSTRACT

In SVPWM technique, the voltage reference provided using revolving reference vector. In this case magnitude and frequency of the fundamental component in line side is controlled by the magnitude and frequency respectively of the reference voltage vector. Space vector modulation techniques utilize the DC bus voltage more efficiently and generate less harmonic distortion when compared to sinusoidal PWM (SPWM) technique. The space vector pulse width modulation control technique has been applied to five level flying capacitor inverter and their performance has been analyzed by using MATLAB /Simulink. The output shows better performance results. The variations based in Total harmonics distortion are also analyzed.
Key words- DC Bus Voltage Utilization, Neutral Point flying Clamped Inverter (NPFCI), Total Harmonic Distortion, Sinusoidal Pulse Width Modulation (SPWM), Space Vector Pulse Width Modulation (SVPWM).

I.INTRODUCTION

The inverters in such application areas as stated above should be able to handle high voltage and large power. For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as gate-turn-off thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors The inverters in such application areas as stated above should be able to handle high voltage and large power. For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching. power devices such as gate-turn-off thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors. The inverters in such application areas as stated above should be able to handle high voltage and large power. For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as gate-turn-off thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors (IGBTs), because the series connection allows reaching much higher voltages. However, the series connection of switching power devices has big problems [13], namely, non-equal distribution of applied device voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices.

Multilevel converters are a very attractive solution for medium-voltage high-power conversion applications; such as motor drives, microgrids, and distributed generation systems. The main features of these topologies, as compared with the two-level voltage-source converters (VSC), are their capabilities to reduce:

1) Harmonic distortion of the ac-side waveforms;

2) dv/dt switching stresses;

3) Switching losses; and

Multilevel inverters have gained interest during the last three decades due to the increasing demand for medium to high voltage converters for a variety of high power applications. Different topologies have been proposed to fit the requirements of different applications. For medium voltage inverters, cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) are the primary topologies. Among them, NPC and FC provide a common dc-link which is a strict requirement for many applications [6]

FC inverter uses capacitors to generate output voltage levels. The availability of intra-phasal redundant states in this topology can provide both capacitor voltage balancing and power loss distribution among switches [7]. However, increased number of flying capacitors at higher levels that increases the initial cost and maintenance surcharges and decreases the reliability of the inverter along with the capacitor precharge in some applications are the main drawbacks of this topology [8].

NPC inverter uses diodes to clamp the voltage levels generated at the dc-link capacitors to the output. Excessive number of diodes, unbalanced operation of dc-link's voltage divider capacitors, and uneven

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distribution of loss among switches are major problems of this topology. Space vector algorithms are available to alleviate the unbalanced loss and capacitor voltage problems based on the inverter's operating condition [5]. Active NPC (ANPC) improves the loss

distribution of NPC by replacing diodes with active switches providing alternative neutral point path [9].

Hybrid topologies are viable solutions where higher number of levels is required. Combining the advantages of CHB, FC, and NPC, hybrid inverters can provide loss and voltage balancing while keeping the number of components low. Examples of hybrid topologies combining FC and NPC can be found in [10]–[12], some of which has already found industrial applications. The 5-level FC-ANPC is an example of hybrid topologies that made its way to the industry. The ACS2000 family of medium voltage drives, commercialized by ABB, uses this topology with both active and passive front end configurations. The main advantage of this topology is the use of a single flying capacitor to generate the output five levels. Compared to other topologies that provide a common dc-link, FC-ANPC has provided an acceptable tradeoff between the cost, performance, and reliability for 5-level applications. The disadvantages of FC-ANPC are high number of switches, series connection of high voltage switches, and poor loss distribution [13].

The proposes a new 5-level hybrid topology based on FC and NPC inverters. The goal of the proposed topology is to overcome the shortcomings of the traditional FC-ANPC. Thus, comparatively, the proposed topology provides better loss distribution, avoids direct series connection of high voltage switches, and eliminates 2 switches per phase leg. These advantages come at the cost of an additional capacitor and 6 diodes. Nevertheless, the lifetime of each capacitor is expected to prolong due to the half cycle operation and lower rms current.

Power electronic researchers have place in continuous efforts in developing topologies that retain the inherent edges of construction inverters with lesser range of power switches and different extra options. With the arrival of latest topologies, a larger stress is additionally placed on to research new switching strategies. This is because of the fact that a particular switching strategy for a given topology can result in improvement of harmonic profile of output waveform as well as reduction in switching and conduction power losses. The three switching methods most discussed in the literature are:

- Carrier-based PWM

- Selective Harmonic Elimination
- Space-vector PWM
- Optimized Harmonic PWM (OHPWM)

1.1 Applications of Multi-Level Inverters

Multilevel converters are well thought-out today as a very attractive resolution for medium-voltage high-power applications.

In fact, many major makers commercialize bureau, FC, or CHB topologies with a large style of management strategies, every one powerfully looking on the appliance. Significantly, the DC inverter has found a crucial market in additional standard dynamical ac motor drive applications like conveyors, pumps, fans, and mills, among others, which provide solutions for industries as well as oil and gas, metals, power, mining, water, marine, and chemistry. The consecutive configuration for regenerative applications has conjointly been a significant and of this topology, used, as an example, in regenerative conveyors for the mining business or grid interfacing of renewable energy sources like wind generation. On the opposite hand, FC converters have found explicit applications for prime bandwidth–high shift frequency applications like medium-voltage traction drives

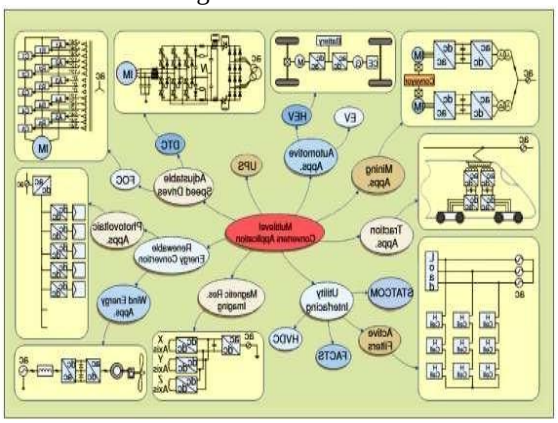

Fig. 1.1 Applications of Multilevel inverters

Finally, the cascaded H-bridge has been with success commercial for high-powered and power-quality rigorous applications up to a spread of thirty one MVA, because of its series enlargement capability. This topology has conjointly been presented for active filter and reactive power compensation applications, electrical and hybrid vehicles, electrical phenomenon power conversion, uninterruptible power provides, and resonance imaging.

II. Proposed Methodology

The proposed topology includes a dc-link that is

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common among the three phases. The dc-link provides three voltage levels +2E, 0, and -2E for the phase legs. Since all the phases have similar configuration, only one phase leg of the proposed topology has been shown in Fig. 2.1. All the components shown in the figure have equal operating voltage E i.e. one fourth of the dc-link voltage V_{dc}. The flying capacitors C_{A1} and C_{A2} are controlled to stay charged at the target voltage E.

The available states of one phase leg are shown in table 4.1. To generate level 2E, all the top arm switches S_{A1}, S_{A2}, S_{A3}, S_{A4} should turn on. For level E, two choices are available i.e. either through dc-link's positive point (EP) or through dc-link's neutral point (E0). This redundancy can be used to balance the voltage of C_{A1}. Level 0 is generated through clamping the dc- link's neutral point to the output (00). Negative states can be generated similarly due to the symmetry of the topology.

The operation of this topology is in essence similar to topologies such as stacked multicell (SMC) converter, where the positive and negative stacks operate independently. Hence, the positive stack capacitor C_{A1} is used and balanced during the positive cycle and rest during the negative cycle, whereas the negative stack capacitor C_{A2} is used and balanced during the negative cycle and rest during the positive cycle. So, the flying capacitors will see the switching frequency rather than line frequency and therefore the capacitor size is not too large.

Similar to the three-level NPC inverter, if the three phases of the load are balanced, the neutral point voltage will be constant in theory. However, the voltage might slightly drift away due to the imbalance in the elements' leakage current. In addition, although small, there is always some imbalance among the phases. A constant voltage drift, even though small, can cause higher voltage across part of the devices which can be lethal. Nevertheless, this drift can be compensated by injecting a small common mode to the three phases.

2.1 MODULATION TECHNIQUES

Various modulation techniques may be adapted for the proposed topology. Carrier-based modulation with sinusoidal or modified reference as well as non-carrier-based techniques such as space vector modulation and selective harmonic elimination may be used to generate the gate signals. The choice of a modulation technique is mostly a tradeoff among the requirements of the application

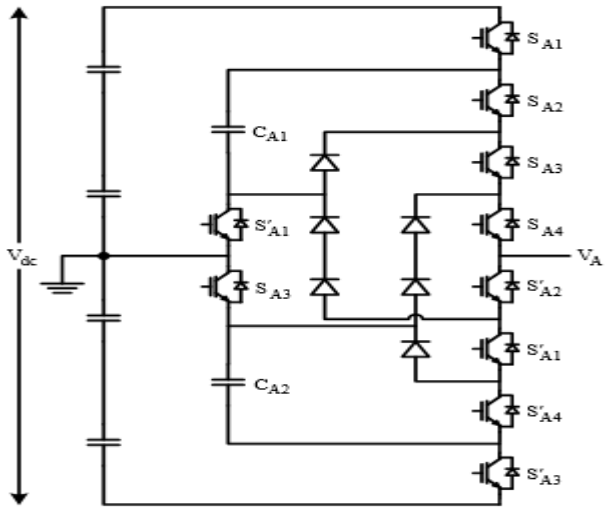

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Fig. 2.1. A phase leg of the proposed 5-level hybrid topology

TABLE 2.1. SWITCHING STATES OF THE PROPOSED INVERTER

Level	State	S2	S3	S4	C1	C2
+2E	+2E	1	1	1	N.A.	N.A.
+E	+EP	0	1	1	i>0 Charge i<0 Discharge	N.A.
	+E0	1	1	1	i>0 Discharge i<0 Charge	N.A.
0	0	0	1	1	N.A.	N.A.
-E	-E0	0	1	0	N.A.	i>0 Charge i<0 Discharge
	-EN	0	0	1	N.A.	i>0 Discharge i<0 Charge
-2E	-2E	0	0	0	N.A.	N.A.

2.3 carrier Modulation

Carrier set's arrangement and reference waveform's shape are the main sources of varieties in carrier-based modulation techniques for multilevel inverters.

As for carrier set's arrangement, level shifted carriers LSC and phase shifted carriers PSC are the two main categories that are respectively suitable for diode-clamped and multi-cell structures. Two members in the LSC family, alternative phase opposition disposition APOD and phase disposition

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PD are known to generate the best results for singe-phase and three- phase applications, respectively. PSC in its original form has been shown to generate a PWM waveform that matches with APOD. Also a modified version of PSC with dynamic phase shift has been shown to match with PD [16].

The reference for single-phase applications is usually a simple sinusoidal waveform. For three-phase applications, a variety of reference waveforms are available due to the possibility of common mode injection in three-phase structure. This flexibility has been used to serve different purposes such as increased dc link utilization, lower THD, lower Loss, and neutral point voltage control.

For three-phase case, similar approach may be adopted except that, to generate a PD scheme equivalent, the positive cycle carriers should have $\pi/2$ phase shift compared to the negative cycle carriers. Also, the carriers incorporate a dynamic phase shift which for sampled reference waveforms always adds up by $\pi/2$ at the carrier band transitions. For the reference waveform, centered space vector PWM (CSVPWM) sampled at half PD carrier period can provide similar output performance as SVM. Figure 4 illustrates the modulation technique using sampled CSVPWM along with modified PSC for the proposed inverter.

2.4 Non-Carrier-Based Modulation

For non-carrier-based modulation techniques such as SVM and SHE, the output PWM waveform may be generated first and then decomposed to the required switching signals. Figure 4 illustrates the required procedure to generate the gate signals for each phase leg. The 5-level PWM waveform is first separated to positive and negative cycle 3-level PWMs. Using stae machine decoder, each cycle is then decomposed to two 2-level PWMs i.e. the required gate signals for each FC cell.

It is important to note that this procedure is independent of the adopted modulation technique. Therefore, it can be used with carrier-based modulation techniques as well as non- carrier-based. This might be a good alternative when the complexity of the carrier-based technique is relatively high e.g. for PD scheme.

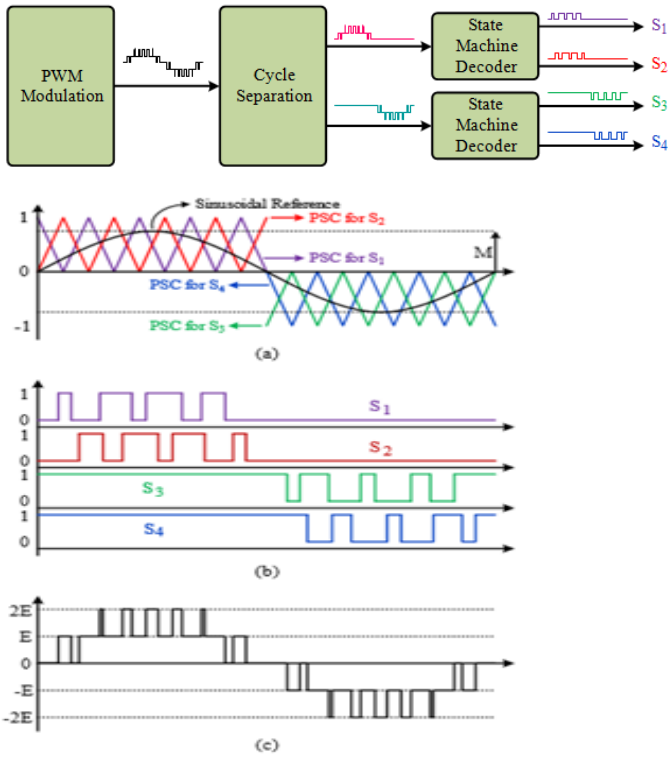

Fig. 2.2. Carrier-based modulation using PSC with sinusoidal reference for single phase

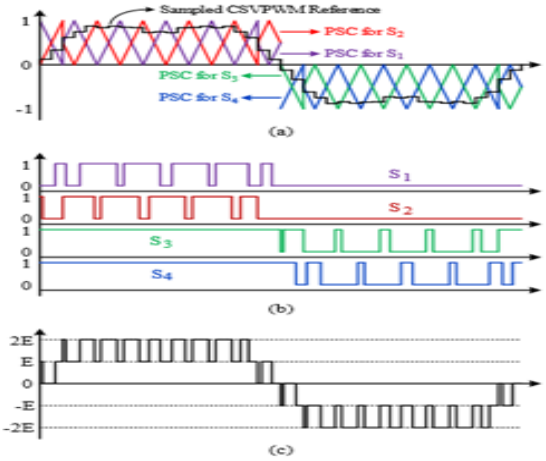

Fig. 2.3. Carrier-based modulation using modified PSC with sampled CSVPWM reference

III. SIMULATION RESULT& DISCUSSION

For validation of proposed work here MATLAB/Simulink based model is shown in figure 3.1and 3.2.

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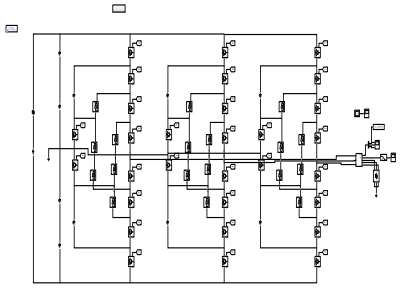

Fig no .3.1 The proposed hybrid active neutral point five level flying capacitor using spwm topology

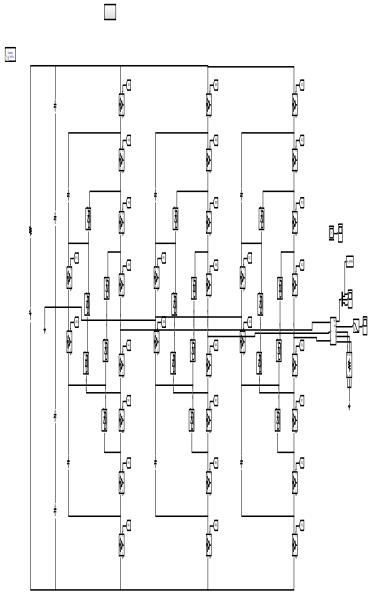

Fig no .3.2 The proposed hybrid active neutral point five level flying capacitor using svpwm topology

The above is the modelling of hybrid active neutral point converter clamped flying capacitor multilevel inverter with three phases. Each phase comprises of 10 IGBTs operating in synchronization with 120 degrees phase delay to each other.

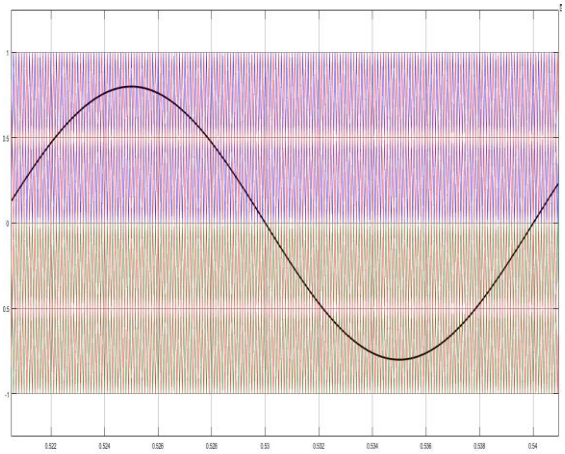

Fig. 3.3 Sinusoidal comparison to high frequency triangular waveform

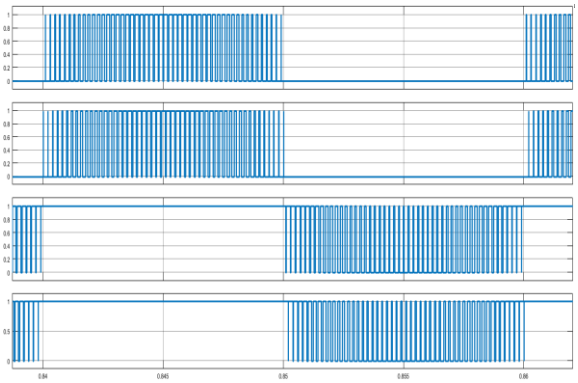

Fig. 3.4 Pulses for the upper region switches

The pulses generated for the upper region switches with comparison of four level shifted high frequency triangular waveforms are connected to NOT gate to generate pulse for lower region switches. The output generated after the pulses are fed to the IGBT switches is shown below.

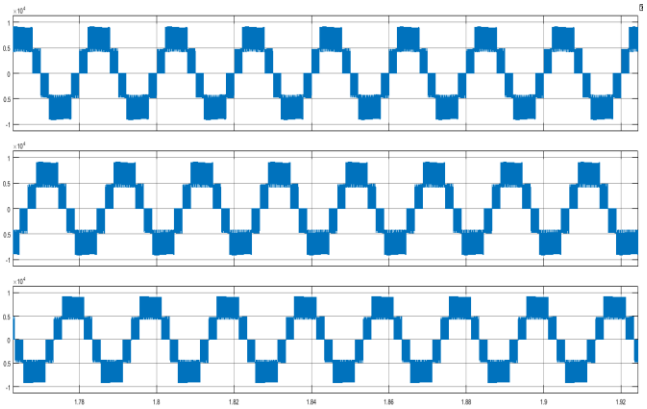

Fig. 3.5 Five level output voltages of phase abc using Sinusoidal PWM technique

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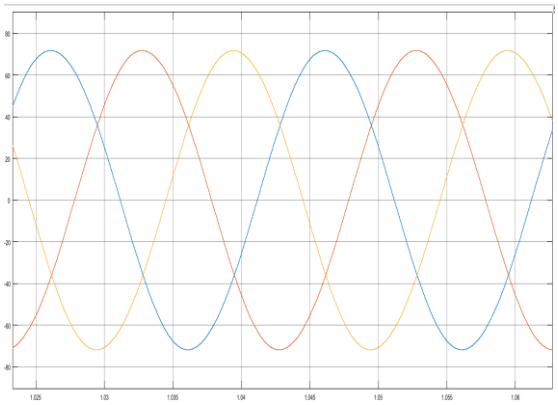

Fig. 3.6 Load current with resistive load in spwm

The modelling is updated with carrier-based space vector PWM technique with no change in the IGBT connections or the topology. The carrier-based space vector PWM is shown below.

The control signals are compared to four level shifted high frequency triangular waveforms generating pulses for upper region switches similar to the previous topology. The output voltages are recorded and compared with the previous topology.

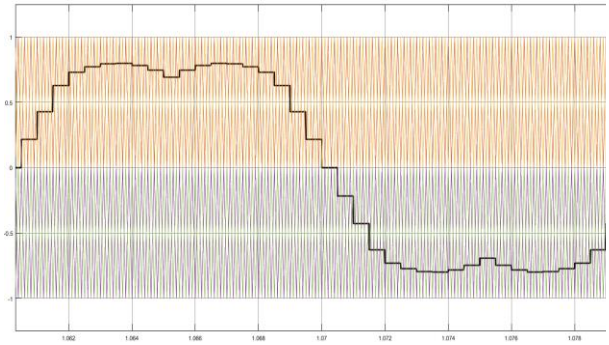

Fig. 3.7 carrier-based space vector PWM technique reference waveforms

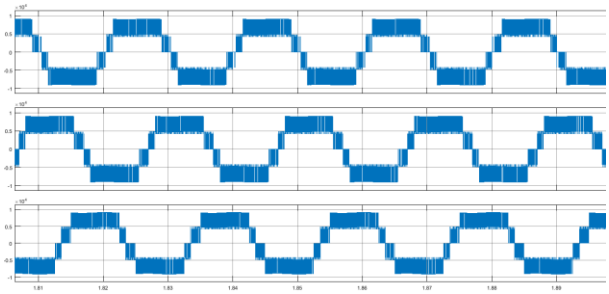

Fig. 3.8 Five level output voltages of phase abc using csv PWM technique

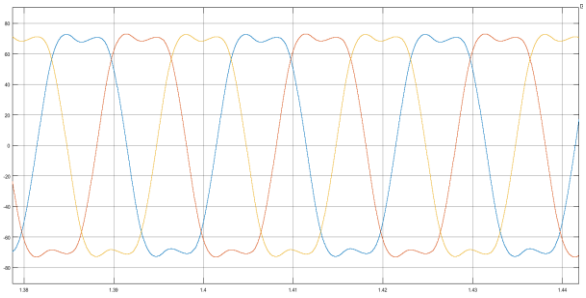

Fig. 3.9 Load current with resistive load in cs pwm

The results are compared using FFT analysis tool for the voltage magnitude and THD of both the voltages with spwm and csv pwm.

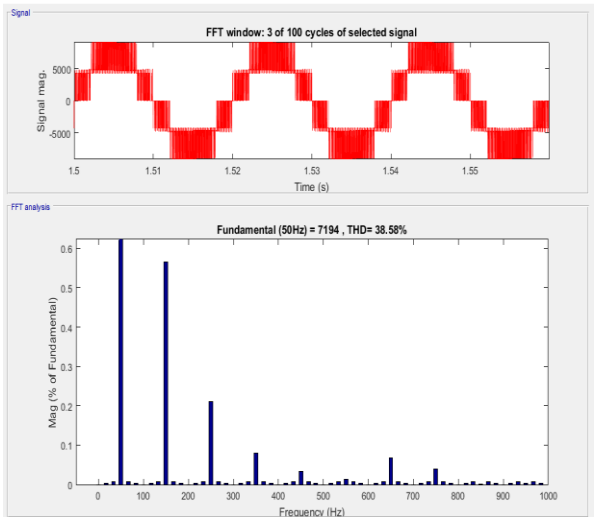

Fig. 3.10 THD of the voltage waveform with spwm technique

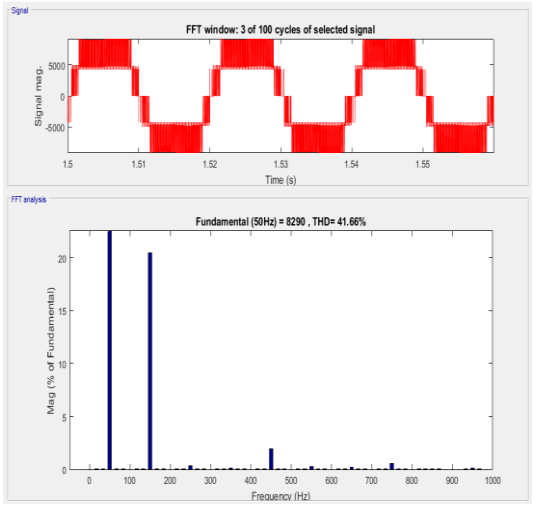

Fig. 3.11 THD of the voltage waveform with csv pwm technique

IV. COCLUSION

Recent trend in power electronics is based on the use of multilevel inverter technology. Multilevel inverter uses so many switches for generating output. Each switch produces loss in the power. This gives low power at the output. So need for some special topology which have low switch. As observed the voltage amplitude of the voltage with spwm technique is recorded at 7194V and for the csv pwm technique it is recorded at 8290 with an increase of approximately 1100V. However, the THD of the csv pwm is analysed at 41.66% and spwm is analysed at 38.58%. which has not much change. The increase of 1100V is considered to be higher change as compared to increase in THD with only 3% increase. The csv pwm technique is more advantageous as compared to spwm with increased voltage amplitude of 1100V and very less increment of THD.

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