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Power Comparison Of Cmos And Full Adder Circuits

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ABSTRACT

Full adders are important components in applications such as digital signal processors (DSP) architectures and microprocessors. Apart from the basic addition adders also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc. In most of these systems the adder lies in the critical path that determines the overall performance of the system. In this paper conventional complementary metal oxide semiconductor (CMOS) and different types of full adder circuits are analyzed in terms of power and delay. A metric to evaluate full adder circuit performance is power delay product (PDP). The driving capability of full adder is very important, because, full adders are mostly used in cascade configuration, where output of one provides the input for others. If full adders lack driving capability then it requires additional buffer which consequently increases the power dissipation.

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KEYWORDS

Low-power, CMOS, Full adder, Pass transistor logic, CMOS Transmission gate, Static Energy Recovery Full adder, Adder9A, Adder9B, channel length, delay.

INTRODUCTION

Power minimization is one of the primary concerns in today VLSI design methodologies because of two main reasons one is the long battery operating life requirement of mobile and portable devices and second is due to increasing number of transistors on a single chip leads to high power dissipation and it can lead to reliability and IC packaging problems.

The low-power requirements of present electronic systems have challenged the scientific research towards the study of technological, architectural and circuital solutions that allow a reduction of the energy dissipated by an electronic circuit.

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The low-power design has become a major design consideration. The design criterion of a full adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery technology has made power consumption an important figure in portable devices.

The speed of the design is limited by size of the transistors, parasitic capacitance and delay in the critical path. The driving capability of a full adder is very important, because, full adders are mostly used in cascade configuration, where the output of one provides the input for other. If the full adders lack driving capability then it requires additional buffer, which consequently increases the power dissipation. In the last decade, the full adder has gone through substantial improvement in power consumption, speed and size, but at the cost of weak driving capability and reduced voltage swing. However, reduced voltage swing has the advantage of lower power consumption .There is no ideal full adder cell that can be used in all types of applications.

One of the main causes of energy dissipation in CMOS circuits is due to the charging and discharging of the node capacitances of the circuits, present both as a load and as parasitic. Such part of the total power dissipated by a circuit is called dynamic power. In order to reduce the dynamic power, an alternative approach to the traditional techniques of power consumption reduction, named adiabatic switching. In such approach, the process of charging and discharging the node capacitances is carried out in a way so that a small amount of energy is wasted and a recovery of the energy stored on the capacitors is achieved.

In this paper, we have given a brief description of the evolution of full adder circuits in terms of lesser power consumption, higher speed and lesser chip size. We have started with the most conventional 28 transistor full adder and then gradually studied full adders consisting of as less as 8 transistors. We have also included some of the most popular full adder cells like Static Energy Recovery Full Adder (SERF), pass transistor logic(PL) based adder, transmission gate(TG) based adder, Adder9A, Adder9B, GDI based full adder.

Adder implementation

A basic cell in digital computing systems is the 1-bit full adder which has three 1-bit inputs (A, B, and C) and two 1-bit outputs (*sum* and *carry*). The relations between the inputs and the outputs are expressed as

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$$SUM = \bar{A}.\bar{B}.C + \bar{A}.B.\bar{C} + A.B.C + A.\bar{B}.\bar{C}$$

$$CARRY = AB+BC+CA$$

Full Adder using CMOS Logic and will be called as "Conventional CMOS design". The block diagram of conventional CMOS is shown in Fig. 1.

TRUTH TABLE OF FULL ADDER

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

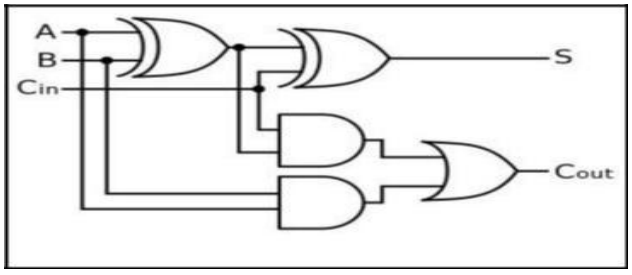

Fig. 1: Block diagram of conventional CMOS

A. CONVENTIONAL 28T CMOS FULL ADDER:

Conventional CMOS Implementation consists of two functional blocks pull-up and pull-down. Pull-up functional block is implemented with P-channel MOS transistors and pull-down functional block is implemented with N-channel MOS transistors. Cout is generated first using equation 3. Then the sum is derived from the sum using equation 4.This adder was based on regular CMOS structure (pull-up and pull-down network) (Fig 2). One of the most significant advantages of this full adder was its high noise margins and thus reliable operation atlow voltages. The layout of CMOS gates was also simplified due to the complementary transistor

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pairs. But the use of substantial number of transistors results in high input loads, more power consumption and larger silicon area.

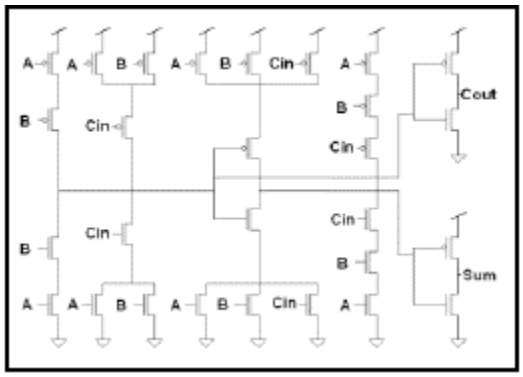

Fig. 2: 28T Conventional CMOS full adder

B. PASS TRANSISTOR LOGIC(PL) BASED ADDER:

Pass transistor logic is one of the well known nMOS logic style used to implement different functions. General method for deriving pass transistor logic diagram for a function is choosing control variable and pass variable based on the functional description. The main concept behind Complementary PL (CPL) is the use of only an nMOSFET network for the implementation of logic functions. This results in low input capacitance and high speed operation. The schematic diagram of the CPL full adder circuit is shown in Fig . Because the high voltage level of the pass-transistor outputs is lower than the supply voltage level by the threshold voltage of the pass transistors, the signals have to be amplified by using CMOS inverters at the outputs. CPL circuits consume less power than conventional static circuits because the logic swing of the pass transistor outputs is smaller than the supply voltage level.

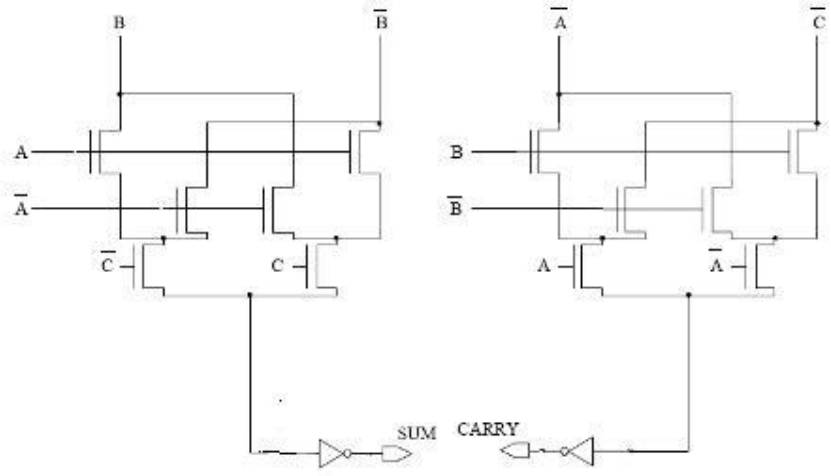

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Fig. : PASS TRANSISTOR LOGIC (PL) BASED ADDER

C. 20 T TRANSMISSION GATE FULL ADDER:

Transmission gate approach is another widely used CMOS design style to implement digital function. Transmission gate based implementation is similar to pass transistor with the difference that transmission gate logic uses nMOS and pMOS transistors where as pass transistor logic uses only one type of transistor i.e. either nMOS or pMOS**.** In the circuit we have 2 inverters followed by two transmission gates which act as 8-T XOR. Subsequently 8-T XNOR module follows. It is the fastest adder so far been reported. The circuit is simpler than the conventional adder. But it produces buffered outputs of proper polarity for both sum and carry with the disadvantage of high power consumption.

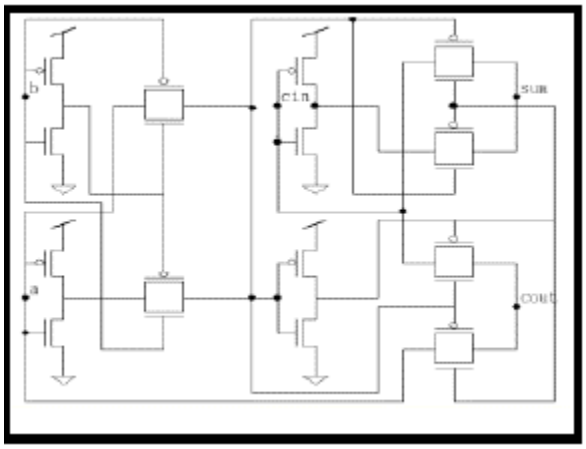

Fig. 3: 20T TRANSMISSION GATE FULL ADDER

D. 14T FULL ADDER:

The 14T full adder contains a 4T PTL XOR gate, shown in Fig. 4, an inverter and two transmission gates based multiplexer designs for sum and Cout signals. This circuit has 4 transistor XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used simultaneously to generate sum and cout. The signals cin and $\overline{\equiv}$ are multiplexed which can controlled either by (a b) or (a $\otimes$ b). Similarly the cout can be calculated by multiplexing a

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andcin controlled by (a b). It is the fastest adder so far been reported. The circuit is simpler than the conventional adder. But the power dissipation in this circuit is more than the 28T adder. However with same power consumption it performs faster .

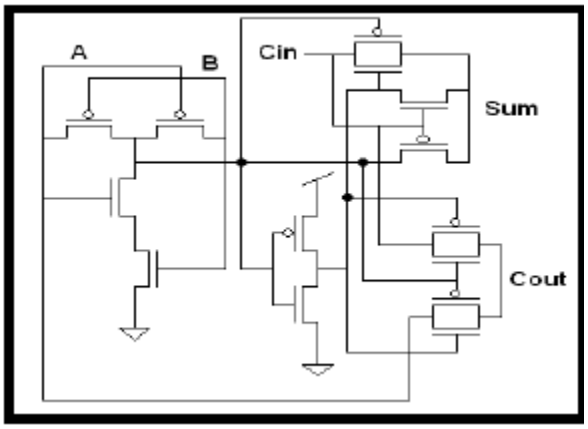

Fig. 4: 14T FULL ADDER

E. 10T STATIC ENERGY RECOVERY FULL ADDER:

In the 10T adder cell, the implementation of XOR and XNOR of A and B is done using pass transistor logic and an inverter is to complement the input signal A. This implementation results in faster XOR and XNOR outputs and also ensures that there is a balance of delays at the output of these gates. This leads to less spurious SUM and Carry signals. The capacitance at the outputs of XOR and XNOR gates is also reduced as they are not loaded with inverter. If the signal degradation at the SUM and Carry is significant for deep sub-micron circuits, drivers can be used to reduce the degradation. The driver will help in generating outputs with equal rise and fall times. This results in better performance regarding speed, low power dissipation and driving capabilities. The output voltage swing will be equal to the V_{DD}, if a driver is used at the output.
In this type of adder (Fig 5) the energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. The circuit consists of two XNORs realized by 4 transistors. Sum is generated from the output of the second stage XNOR circuit. The cout can be calculated by multiplexing **a** and $\mathbf{c_{in}}$ controlled by ($\mathbf{a \otimes b}$). The energy consumption is low here
It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to the ground reduces power consumption. The charge stored at the load capacitance is

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reapplied to the control gates. The combination of not having a direct path to ground and the re-application of the load charge to the control gate makes the energy-recovering full adder an energy efficient design.

The circuit produces full-swing at the output nodes. But it fails to provide so for the internal nodes. As the power consumption by the circuit reduces the circuit becomes slower. Also it cannot be cascaded at low power supply due to multiple threshold problems.

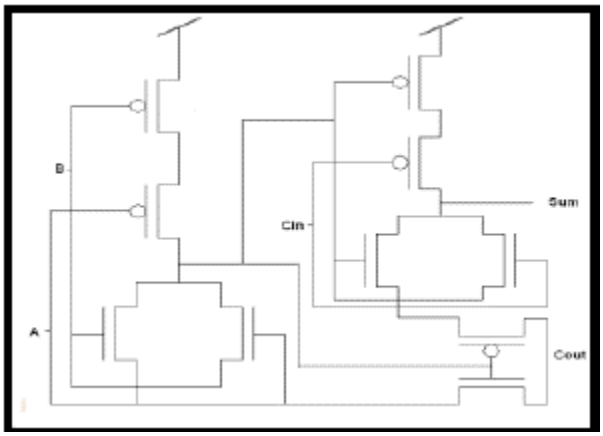

Fig. 5: 10T STATIC ENERGY RECOVERY FULL ADDER

F. 10T FULL ADDERS REALIZED BY GATE DIFFUSION INPUT (GDI) STRUCTURES:

Now using these GDI based XOR and XNOR gates two different GDI based full adder architecture were designed [Fig. 6]. **:** The circuit operation of GDI Based Full Adders is exactly the same as that of previous SERF module. Sum bit is obtained from the output of the second stage of XOR [Fig. 6(a)], XNOR [Fig. 6(b)] circuit while Carry bit (Cout) is calculated by multiplexing B and C_{in} controlled by (A XNOR B).

These features give the GDI cell two extra input pins to use which makes it flexible than usual CMOS design. It is also a genius design which is very power efficient without huge amount of transistor count.

The major problem of a GDI cell is that it requires twin-well CMOS or silicon on insulator (SOI) process to realize. Thus, it will be more expensive to realize a GDI chip. Moreover if only standard p-well CMOS process is used, the GDI scheme will face the problem of lacking driving capability which makes it more expensive and difficult to realize as a feasible chip.

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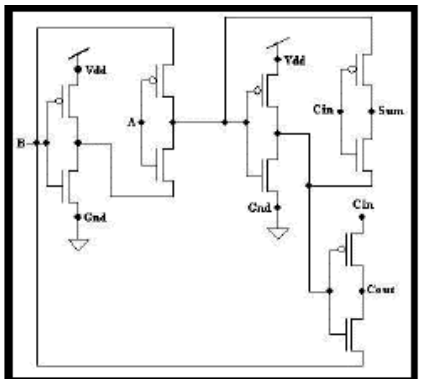

Fig. 6(a)

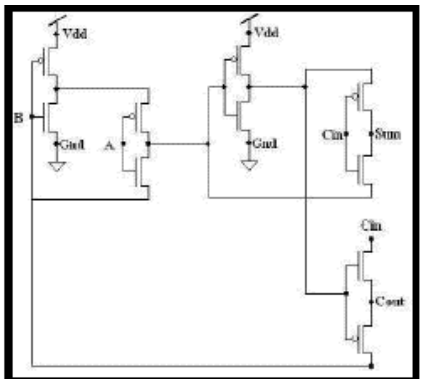

Fig. 6(b)

Fig. 6: 10T FULL ADDERS REALIZED BY GATE DIFFUSION INPUT (GDI)

G. ADDER 9A AND 9B:

From the above figures (Fig 7a and 7b), we can see that a Static Energy Recovery XNOR gate is cascadedwith the new G-XNOR gate to generate the Sum while the Cout function is implemented by simply multiplexing B and Cin controlled by (A XNOR B) as done in the previous circuits.

These two new adders consistently consume less power in high frequencies and have higher speed compared with the previous 10-transistor full adders and the conventional 28-transistor CMOS adder.

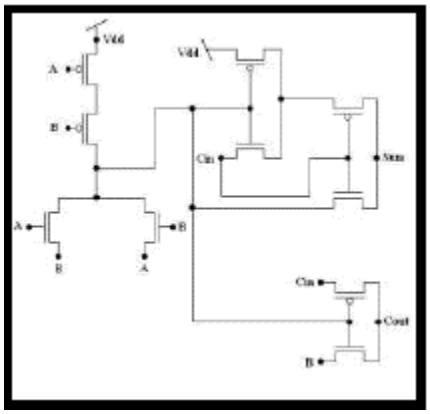

Fig. 7(a): Adder9A

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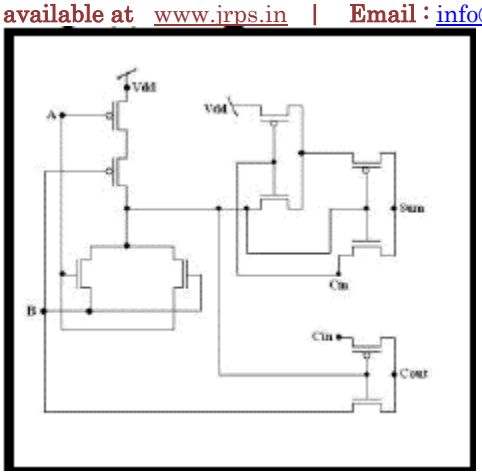

Fig. 7(b): Adder9B

H. DESIGN OF 8T FULL ADDER:

The basic of 8T full adder consists of 3 modules: 2 XOR elements and a Carry section as shown in figure 8.

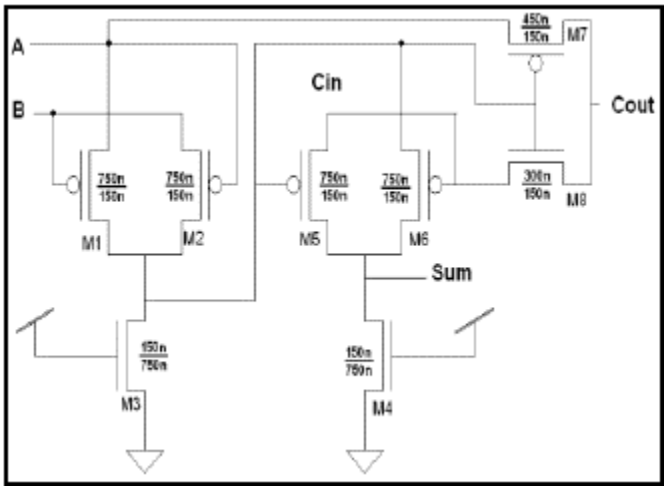

Fig. 8: 8T FULL ADDER

The Sum output is obtained by two XOR blocks in succession. For the carry section we use GDI based 2T-MUX and (A XOR B)as the selection signal. The Sum and the Cout module need 6 and 2 transistors respectively. The transistor level implementation of the eight transistor full adder is shown in Fig. 8. Advantage is obvious from the figure that both Sum and Cout has a maximum delay of 2T. It doesn't suffer from threshold voltage loss problem. Also the noise margin has been substantially increased byproper sizing of transistors in 3T XOR. The power delay product

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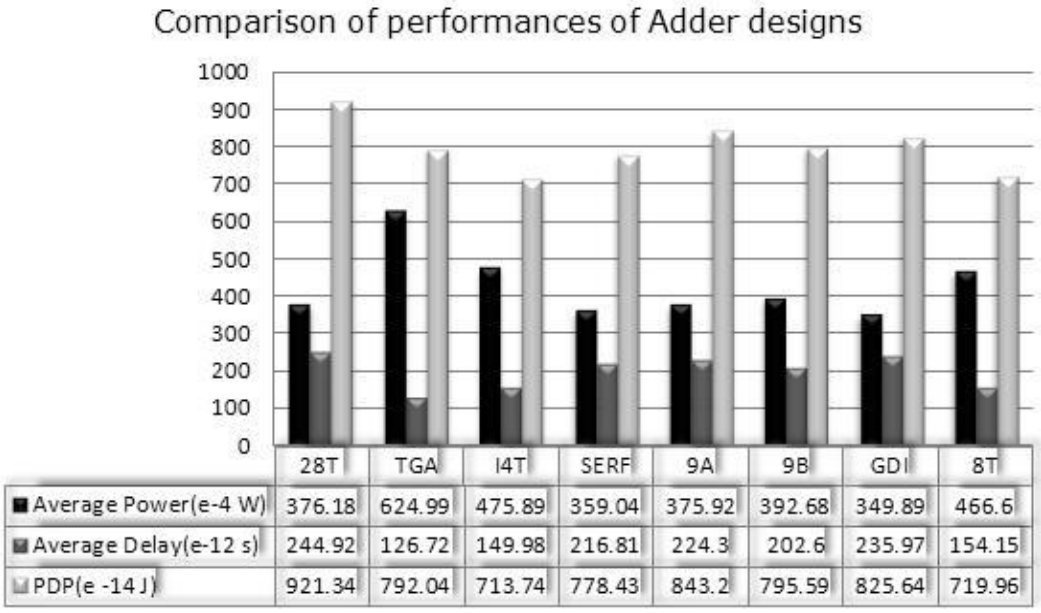
(PDP), and the area of the proposed adder are also found better than that of the existing 10T and 14T adders. But the higher power consumption due to short circuit current.

Result:-

Comparative analysis between various type of full adder is shown in Fig. 9



	28T	TGA	I4T	SERF	9A	9B	GDI	8T
Average Power(e-4 W)	376.18	624.99	475.89	359.04	375.92	392.68	349.89	466.6
Average Delay(e-12 s)	244.92	126.72	149.98	216.81	224.3	202.6	235.97	154.15
PDP(e -14 J)	921.34	792.04	713.74	778.43	843.2	795.59	825.64	719.96

Fig. 9: comparative analysis of different types of full adder

Conclusion:-

From the analysis of the above various type of Full Adder Circuits we can reach to a conclusion that the average power is low for GDI type Full adders and Average Delay is low for TG Based Full Adder. But the Power Delay Product is low for 14T Full Adder. But Power dissipation is higher than 8T Full Adder. For Optimization of Power (Average power) and Delay, we think that the best option is 8T Full Adder.

Full Adders is the heart of any digital processor. Here we have shown the implementation of various type of Full Adders using MOSFET. However recent researches have shown that Carbon-Nano Tubes have a huge potential in logic circuits. Not only will it reduce power consumption, but also increase speed substantially.

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