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SIMULATION OF POWER CONSUMPTION AND QUALITY OF HYBRID MULTIPLIER

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Abstract: It has been observed that it not simple to develop the digital systems. The objective of Proposed work is split into convenient subunits building blocks with the use of well-organized and efficient designers in any field. After that they utilize the standard subunits where there are acceptable. The building blocks used in proposed work would be adders, registers, and multiplexers in digital hardware. It is presented by the logic theory that all digital operations may be reduced to elementary logic functions. This paper use MATLAB as simulation tool in order to perform comparative analysis of traditional and proposed work. Simulation considers the influencing factors cost factor, power consumption factor, quality factor, mass production factor, pollution factor.

Keyword: Multiplier, Fractional Product Array, Multiplier Reduction Tree, Twin Precision Magnus

[1] INTRODUCTION

It is not easy to create the digital systems. The original work is split into convenient subunits building blocks with the use of well-organized and efficient designers in any field. After that they utilize the standard subunits where there are acceptable. The building blocks are known as adders, registers, and multiplexers in digital hardware. It is presented by the logic theory that all digital operations may be reduced to elementary logic functions. We will considered that a digital system made by the use of massive group of and, or, and not circuits. However incomprehensible outcomes are obtained. To resolve this problem it is required to shift 1 level up from the concept of gates.

If a comparison is made between addition and Multiplication it is come in to notice that the latter is a vital fundamental arithmetic operation and less common operation with respect to addition. However it is crucial for microprocessors, digital signal processors and graphic engines. The demonstration of methods which are used for the design of different cells so that they fit into a larger structure is done by the use of Multiplication algorithms. A series of addition, subtraction and shift operations is performed for the execution of multiplication. It is very costly and slow operation. To resolve the problem of speed a high speed multiplier is used from which high speed multiplication is obtained. It is one of the fundamental functions deployed in digital signal processing (DSP). In comparison to addition and subtraction more hardware resources and processing time is required in multiplication function. An usual CPU gives a substantial amount of processing time for the realisation of arithmetic operations in computers, particularly multiplication operations.

Multiplier

A multiplier is a hardware circuit dedicated to multiply 2 binary numbers are multiplied by the use of a hardware circuit which is known as multiplier. For the realisation of a digital multiplier a range of computer arithmetic methods can be used. Firstly the computing of a bundle of fractional products is done and after that fractional products are summing together in almost each and every method. It is related to the process which is used for the student of junior classes for conducting long multiplication on base-10 integers.

Multiplication dominates the implementation time of most DSP algorithms is depends upon the multiplication. Therefore the requirement of high speed multiplier is essential. Most high for the realization of high data throughput all the DSP system whose performance are good have faith in hardware multiplication. Multiplication is an important fundamental arithmetic operation. The multiplier is a fairly large block of a computing system. The quantity of circuitry implicated is directly proportional to quarrel of its resolution i.e., a multiplier of size of n bits has O (n2) gates.

There are two different methods of multiplication algorithms, serial multiplication algorithms and parallel

Multiplication algorithms: Serial multiplication algorithms utilize chronological circuits with feedbacks. In this algorithm, internal commodities are consecutively formed and computed. Parallel multiplication algorithms frequently bring into play combinational circuits and do not control feedback structure. In earlier times, plethoras of novel facts for multipliers were projected to reach high presentation. The command in support of high pace processing is escalating as a result of

growing computer and indicator processing applications. Advanced throughput arithmetic behaviours are vital to attain the needed presentation in various real-time indicator and picture processing applications. One of the key arithmetic actions in such applications is duplication and the progress of rapid multiplier circuit has been a matter of concern over decades. Falling the period hold-up and power utilization are very necessary desires for various applications.

[2]LITERATURE REVIEW

Modified Booth Multipliers With a expected Fractional Product Array. Shiann-Rong Kuang et al (2009) : an uneven fractional product array is accomplished by the usual modified Booth encoding (MBE).It happens due to the presence of the additional fractional product bit at the slightest considerable bit position of all fractional product row. **Multiplication Acceleration Through Twin Precision Magnus. Själander et al (2009) : t**he twin-precision procedure for integer multipliers is put forward by us. Power dissipation can be cut by the use of this procedure. It can be done the by accommodate a multiplier to the bit width of the operands being figure out. A better computational throughput is making possible by the use of this procedure. It is possible because this procedure allows us the parallel operation of a number of narrow-width operations which are to be figure out.

Multiplier Reduction Tree with Logarithmic Logic Depth and Regular connectivity: H Ericsson et al (2006) : For utilizing the I integer multiplication is fresh partial product reduction circuit is put forward. The high performance multiplier (HPM) reduction tree has th 6 of layout of a simple carry save reduction array.

Implementation of a High speed Multiplication on SOC using Twin precision process. G. Swapnasri et al (2012) : for digit multipliers the twin-precision procedure is put forward by us. Power dissipation can be cut by the use of this procedure. It can be done the by accommodate a multiplier to the bit width of the operands being figure out. A better computational throughput is making possible by the use of this procedure. It is possible because this procedure allows us the parallel operation of a number of narrow-width operations which are to be figure out.

High-Speed and Low-Power Multipliers Using the Baugh-Wooley Algorithm and HPM Reduction Tree. Magnus Sjalander et al (2008) : In high-speed multiplier circuits the method of modified-Booth is comprehensively used. A considerably superior performance of multiplier can be achieved by generating the reduced no. of fraction products with the use of array multipliers. The effect of reduced number of fractional products on overall performance is finite in models which uses reduction trees with logarithmic logic depth . The method of Baugh-Wooley algorithm is unusual for signed multiplication.

Performance comparison review of Radix-based multiplier designs. Kelly Liew Suet Swee , Lo Hai Hiung et al (2012) : the present review has been presented a related performance with compare to Radix-based Booth Encoding multiplier. Four Multipliers are involved at the time of making comparison. These are Radix-2 Booth Encoding multiplier, Radix-4 Booth Encoding multiplier, Radix-8 Booth Encoding multiplier, Radix-16 Booth Encoding multiplier and Radix-32 Booth Encoding multiplier. The design of all these multiplier has been altered in Verilog HDL. That has created with dependence on TSMC 0.35-micron ASIC Design Kit standard cell library.

High Speed Modified Booth Encoder Multiplier for Signed and Unsigned Numbers. Ravindra P. Rajput , M.N. Shanmukha Swamy et al (2012) : the present review proposed the implementation and design of SUMBE multiplier. This MBE multiplier and the Baugh-Wooley multiplier have their performance of multiplication operation on signed numbers merely. On the other side, the array multiplier and Braun array multipliers have their performance of multiplication operation merely on unsigned numbers.

Design of modified low power booth multiplier. A. S. Prabhu , Bannari Amman, Sathyamangalam, , V. Elakya et al (2012) : The design of normal multiplier has consumed mostly energy in DSP processors. For decrement of the energy utilization of multiplier, the low power Booth recoding technology has been presented with recoding methodology. That booth decoder has the capability to enlarge the zeros number in multiplicand. Booth multiplier includes the booth decoder for recoding of provided input to booth equivalent.

Design and implementation of high speed modified booth multiplier using hybrid adder. Divya Govekar, Ameeta Amonkar et al (2017) : nowadays the Multiplier has become very required element in mostly designed processors. The multiplier speed decides the processor speed. As a result the high speed multiplier has been required. This review has presented an innovative technique for Multiplication with combination of Modified Booth algorithm, Wallace tree architecture and Hybrid adder design. Modified Booth Multiplier has the power to decrease the partial products number. It has less latency making comparison to other multiplier designs. Wallace Tree makes increment in the speed with parallel adding of partial products.

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Design of an Efficient High Speed Radix-4 Booth Multiplier for both Signed and Unsigned Numbers. D. Kalaiyarasi , M. Saraswathi et al (2018) : the present review shows the blueprint of proficient High speed Radix-4 Booth multiplier. It is in both cases signed as well as unsigned numbers. The Presented Booth multiplier has been considered the multiplier that is efficient. It handles positive as well negative number regularly that has no similarity with conventional multiplier. Often multiplication can be executed through add and shift operation. In this every multiplier bit formulates one multiple bit of the multiplicand. It has addition to the partial product. The multiplicand larger number has addition in case of multiplier larger size.

[3] MULTIPLIERS

A device which is used for the multiplication of 2 binary values is known as multiplier. A digital multiplier put into practice by the use of mixture of computer arithmetic method. Firstly computing of a bundle of fractional products is done in most of the methods. After that summing the fractional products together, further researches are done so that we are able to propose multipliers from which we will get high speed or low power consumption or minimize area.

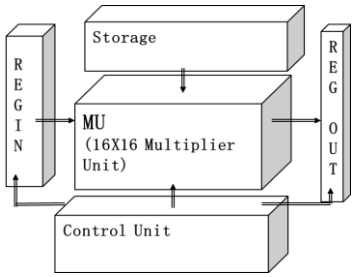

Figure 1: Multiplier Design [16]

If a comparison is made between addition and multiplication it is found that the latter one is an essential basic arithmetic operation but it is less common operation with respect to addition. However it is still required for microprocessors, digital signal processors and graphic engines.
Multiplication algorithms is use to illustrate methods of designing different cells so that they fit into a larger structure. Multiplication is sensibly carried away by a series of addition, subtraction and shift operations. It is a costly and slow operation. So, high speed multiplication has been achieved by having a high speed multiplier.

Multiplication is a mathematical process that at its simplest is a shortened procedure of adding a numeral to itself a specified number of periods. A number (multiplicand) is added to itself an integer of times as precise by other number (multiplier) to shape a result (product). The multiplicand is multiplied with each digit of the multiplier opening with the rightmost, LSD. Transitional results (partial-products) are placed one atop the erstwhile, offset by single digit to support digits of the equal mass. The final product is resolute by outline of all the partial-products. Multiplication takes three main steps:

- Partial product generation
- Partial product reduction
- Final addition

[4] TOOL AND TECHNOLOGY

Matlab

Matlab is known as Language of Technical Computing. It is considered as a high-level language with interactive environment. Matlab enables us to perform computationally tasks quicker as compare to other programming languages such as C, C++, & FORTRAN.
Matrix is a rectangular array of numbers in MATLAB environment. Its Meaning is attached to 1x1 matrices. These are scalars. In order to matrices with one row or column there are vectors. The MATLAB has different ways to store numeric & nonnumeric data. It is best to consider everything as a matrix in beginning. Operations in MATLAB have been designed to be natural. Programming languages other than Matlab work with numbers one at a time but MATLAB offers to work with complete matrices quickly & easily.

[5] RESULT & DISCUSSION

Factor description

Cost factor is C
If cost factor is less then efficiency increases & if cost factor is more than efficiency decreases
Power consumption factor is P
If power consumption factor is less then efficiency increases & if power consumption factor is more than efficiency decreases
Quality Factor is Q
If Quality Factor is less then efficiency decreases & if Quality Factor is more than efficiency increases
Mass Production factor is M
If Mass production factor is less then efficiency decreases & if Mass production Factor is more than efficiency increases
Pollution factor U
If Pollution factor is less then efficiency increases & if Pollution Factor is more than efficiency decreases
Number of Devices is N here
Equation for efficiency E is as follow
E=N (Q+M-P-U-C)
Matlab based GUI design for comparative analysis between traditional & proposed based devices.

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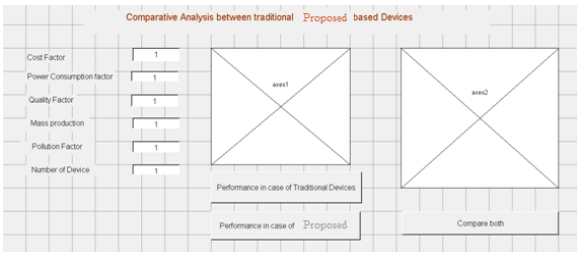

Fig 2. Pollution factor U

Case 1: Cost factor is 1, power consumption factor 1, quality factor is 1.2, mass production factor is 1.1, pollution factor is 1 & number of device is 10.

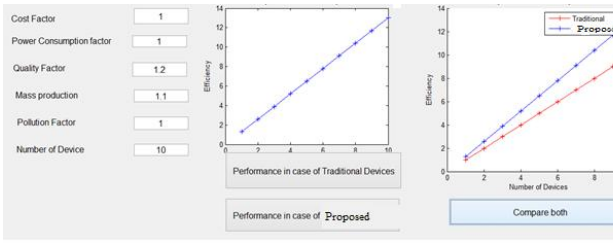

Fig 3. Cost factor is, power consumption factor

Case 2: Cost factor is 0.7, power consumption factor 0.8, quality factor is 1.2, mass production factor is 1.1. Pollution factor is 0.9 & number of device is 10.

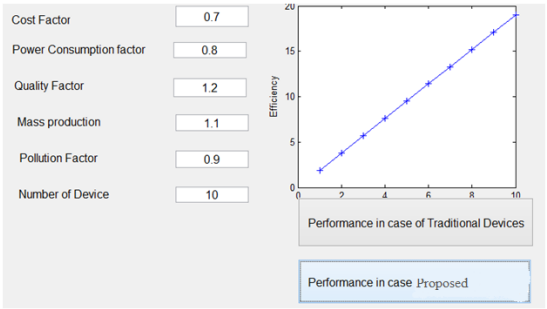

Fig 4. Cost factor is 0.7, power consumption factor

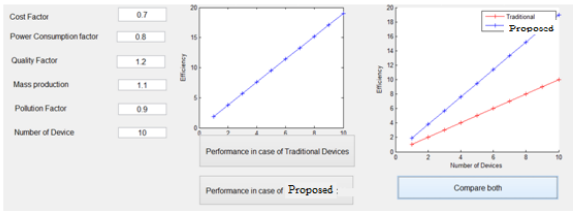

Fig 5. Comparative Analysis between & Proposed based device

Case 3: Cost factor is 0.7, power consumption factor 0.65, quality factor is 1.1, mass production factor is 1.2, pollution factor is 0.6 & number of device is 20.

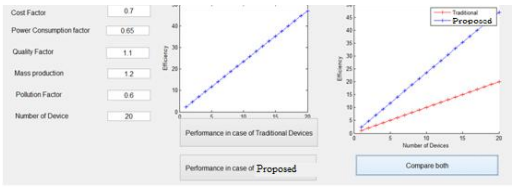

Fig 6. Comparative Analysis between & Proposed based device

[6] Conclusion

The architecture form of 16 X 16 bit manipulated radix-4 booth multiplier and relative evaluation had been occurred.

The design is presented with the use of Verilog-HDL code and effectively simulated on Xilinx ISE 13.4 Synthesis device.

The maximum combinational path that has delay for 16 X 16 bit for manipulated radix-4 booth multiplier is 30.887 ns. The research output has an indication. The manipulated radix-4 booth multiplier offers provide 8.75% enhance the speed have comparison with basic paper output [1].

Sector evaluation as Slices=296, & LUTs=530, the testing output point out that manipulated radix-4 booth multiplier done 57.51 percent less sector as compare to basic paper output [1].

Thus, it has a conclusion that speed of manipulated radix-4 booth multiplier is high and less sector as compare to basic paper output [1].

Thus, Modified radix-4 booth multiplier has been applied in case of high-speed function.

[7] FUTURE SCOPE

As an attempt to develop, arithmetic algorithm and architecture level optimization techniques for high-speed multiplier design. The mechanisms given in this paper has obtained its objectives. On the other side, some restrictions are also placed in this research. The future research directions may be as follows:

One feasible direction is radix higher-as compare to-4 recoding. Only radix-4 recoding has been determined in our work due to its simplicity and acceptance. Higher-radix recoding further decreases the amount of PPs. Therefore it has the ability of energy securing.

To increase the efficiency, higher order compressors such as 7:2, 9:2 have the ability to mount up the partial commodities.

The efficiency of made up small high performance multipliers allows several another attractive feasibilities. Multiplication exhaustive functions, like DSP or graphics, have the ability to obtain the characteristics essentially from numerous high performance multipliers on similar chip. A single that is very high throughput multiplier and various multipliers have execution paralleling one similar chip. Those have the efficiency to open up innovative chances like single chip video signal processors.

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